# CD4011A, CD4012A, CD4023A Types

# CMOS NAND Gates

Quad 2 Input – CD4011A
Dual 4 Input – CD4012A
Triple 3 Input – CD4023A

The TI-CD4011A, CD4012A, and CD-4023A NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of CMOS gates.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

*Features:*

- Quiescent current specified to 15 V
- Maximum input leakage of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

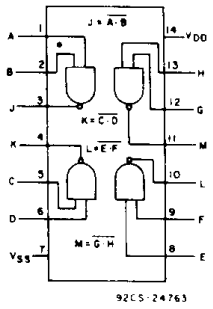
**RECOMMENDED OPERATING CONDITIONS**

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

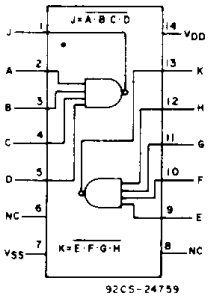
| Characteristic | Min. | Max. | Units |
|---|---|---|---|
| Supply Voltage Range (over full package temperature range) | 3 | 12 | V |

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

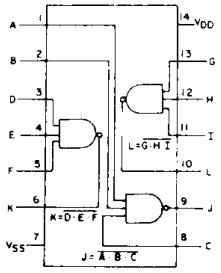
STORAGE-TEMPERATURE RANGE ($T_{stg}$) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE ($T_A$):
  PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
  PACKAGE TYPE E . . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
  (Voltages referenced to $V_{SS}$ Terminal) . . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE ($P_D$):
  FOR $T_A$ = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
  FOR $T_A$ = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
  FOR $T_A$ = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
  FOR $T_A$ = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to $V_{DD}$ +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C




CD4011A

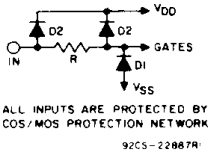



CD4012A




CD4023AH

*Fig. 1 – Functional diagrams.*



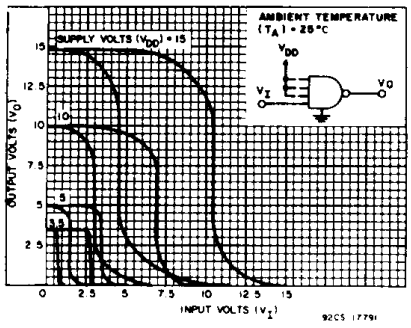




*Fig. 2 – Minimum & maximum voltage transfer characteristics.*

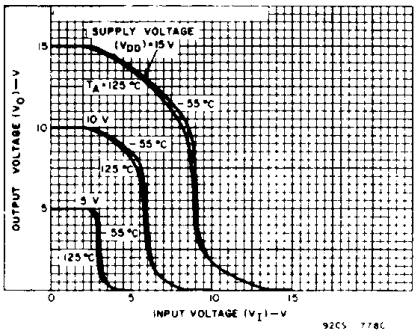



*Fig. 3 – Typical voltage transfer characteristics as a function of temperature.*

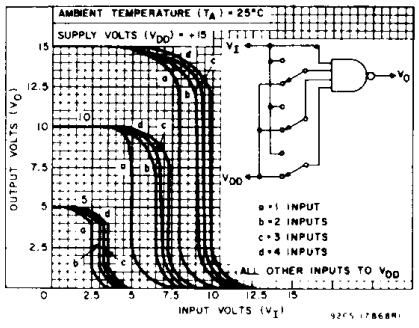



*Fig. 4 – Typical multiple input switching transfer characteristics for CD4012A.*

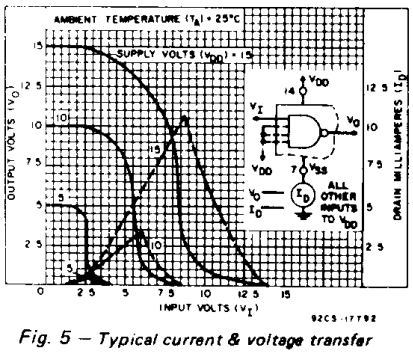



*Fig. 5 – Typical current & voltage transfer characteristics.*

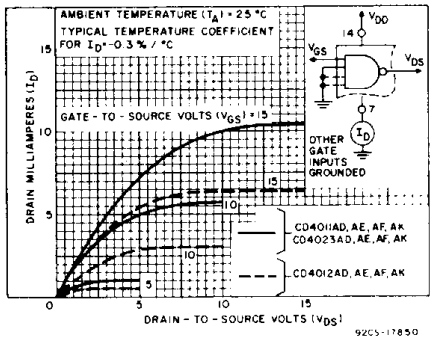



*Fig. 6 – Typical n-channel drain characteristics.*

## STATIC ELECTRICAL CHARACTERISTICS

| Characteristic | Conditions | | | Limits at Indicated Temperatures (°C) | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D,F,K,H Packages | | | | E Package | | | | |
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | −55 | +25 Typ. | +25 Limit | +125 | −40 | +25 Typ. | +25 Limit | +85 | |
| Quiescent Device Current, $I_L$ Max. | – | – | 5 | 0.05 | 0.001 | 0.05 | 3 | 0.5 | 0.005 | 0.5 | 15 | μA |
| | – | – | 10 | 0.1 | 0.001 | 0.1 | 6 | 5 | 0.005 | 5 | 30 | |
| | – | – | 15 | 2 | 0.02 | 2 | 40 | 50 | 0.5 | 50 | 500 | |
| Output Voltage: Low-Level $V_{OL}$ | – | 0,5 | 5 | 0 Typ.; 0.05 Max. | | | | | | | | V |
| | – | 0,10 | 10 | 0 Typ.; 0.05 Max. | | | | | | | | |
| High Level, $V_{OH}$ | – | 0,5 | 5 | 4.95 Min.; 5 Typ. | | | | | | | | |
| | – | 0,10 | 10 | 9.95 Min.; 10 Typ. | | | | | | | | |
| Noise Immunity: Inputs Low, $V_{NL}$ | 3.6 | – | 5 | 1.5 Min.; 2.25 Typ. | | | | | | | | V |
| | 7.2 | – | 10 | 3 Min.; 4.5 Typ. | | | | | | | | |
| Inputs High, $V_{NH}$ | 1.4 | – | 5 | 1.5 Min.; 2.25 Typ.; | | | | | | | | |
| | 2.8 | – | 10 | 3 Min.; 4.5 Typ. | | | | | | | | |
| Noise Margin: Inputs Low, $V_{NML}$ | 4.5 | – | 5 | 1 Min. | | | | | | | | V |
| | 9 | – | 10 | 1 Min. | | | | | | | | |
| Inputs High, $V_{NMH}$ | 0.5 | – | 5 | 1 Min. | | | | | | | | |
| | 1 | – | 10 | 1 Min. | | | | | | | | |
| Output Drive Current: N-Channel (Sink) $I_DN$ Min. CD4011A | 0.5 | – | 5 | 0.31 | 0.5 | 0.25 | 0.175 | 0.145 | 0.5 | 0.12 | 0.095 | mA |
| CD4023A | 0.5 | – | 10 | 0.62 | 0.6 | 0.5 | 0.35 | 0.3 | 0.6 | 0.25 | 0.2 | |
| CD4012A | 0.5 | – | 5 | 0.15 | 0.25 | 0.12 | 0.085 | 0.072 | 0.25 | 0.06 | 0.05 | |
| | 0.5 | – | 10 | 0.31 | 0.6 | 0.25 | 0.175 | 0.155 | 0.6 | 0.13 | 0.105 | |
| P-Channel (Source), $I_DP$ Min. All Types | 4.5 | – | 5 | -0.31 | -0.5 | -0.25 | -0.175 | -0.145 | -0.5 | -0.12 | -0.095 | |
| | 9.5 | – | 10 | -0.75 | -1.2 | -0.6 | -0.4 | -0.35 | -1.2 | -0.3 | -0.24 | |
| Input Leakage Current, $I_{IL}$, $I_{IH}$ | Any Input | | 15 | $\pm 10^{-5}$ Typ.; ±1 Max. | | | | | | | | μA |

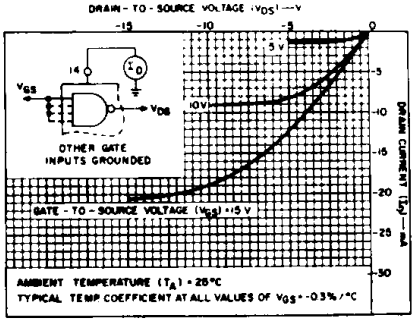



*Fig. 7 — Typical p-channel drain characteristics.*

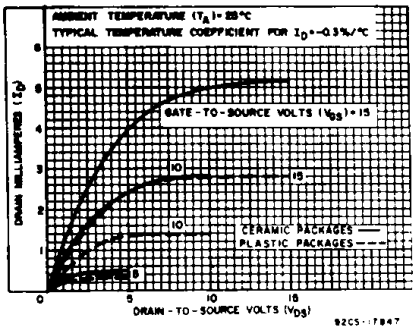



*Fig. 8 — Minimum n-channel drain characteristics —CD4011A & CD4023A.*

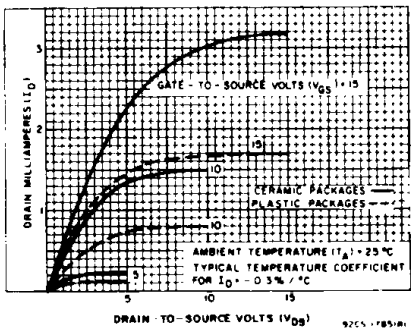



*Fig. 9 — Minimum n-channel drain characteristics.*

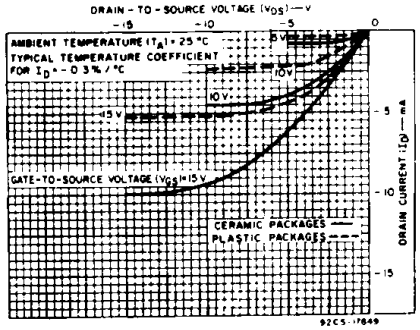



*Fig. 10 — Minimum p-channel drain characteristics.*

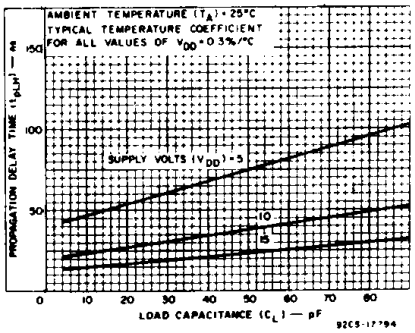



*Fig. 11 — Typical low-to-high level propagation delay time vs. $C_L$.*

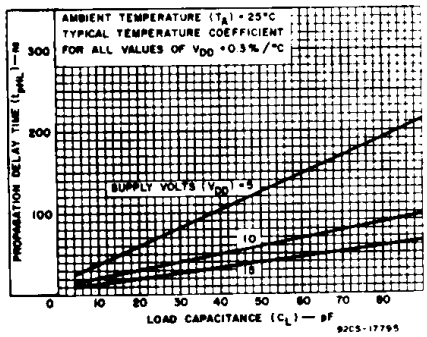



*Fig. 12 — Typical high-to-low level propagation delay time vs. $C_L$ — CD4011A, & CD4023A.*

# CD4011A, CD4012A, CD4023A Types

**DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A$ = 25°C, $C_L$ = 15 pF, Input $t_r$, $t_f$ = 20 ns, $R_L$ = 200 KΩ**

| CHARACTERISTICS | TEST CONDITIONS | | LIMITS | | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | D, F, K, H Packages | | E Package | | |
| | | $V_{DD}$ (V) | Typ. | Max. | Typ. | Max. | |
| Propagation Delay Time: Low-to-High Level, $t_{PLH}$ | | 5 | 50 | 75 | 50 | 100 | ns |
| | | 10 | 25 | 40 | 25 | 50 | |
| High-to-Low Level, $t_{PHL}$ CD4011A and CD4023A | | 5 | 50 | 75 | 50 | 100 | ns |
| | | 10 | 25 | 40 | 25 | 50 | |
| CD4012A | | 5 | 100 | 150 | 100 | 200 | ns |
| | | 10 | 50 | 75 | 50 | 100 | |
| Transition Time: Low-to-High Level, $t_{TLH}$ | | 5 | 75 | 100 | 75 | 125 | ns |
| | | 10 | 40 | 60 | 40 | 75 | |
| High-to-Low Level, $t_{THL}$ CD4011A and CD4023A | | 5 | 75 | 125 | 75 | 150 | ns |
| | | 10 | 50 | 75 | 50 | 100 | |
| CD4012A | | 5 | 250 | 375 | 250 | 500 | ns |
| | | 10 | 125 | 200 | 125 | 250 | |
| Input Capacitance, $C_I$ | Any Input | | 5 | – | 5 | – | pF |

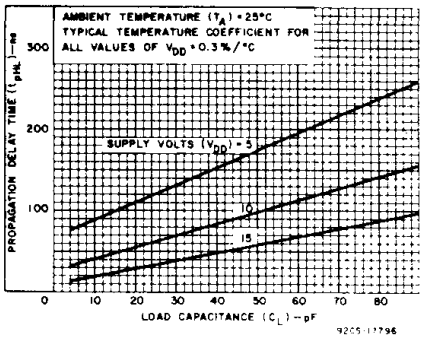



*Fig. 13 – Typical high-to-low level propagation delay time vs. $C_L$ – CD4012A.*

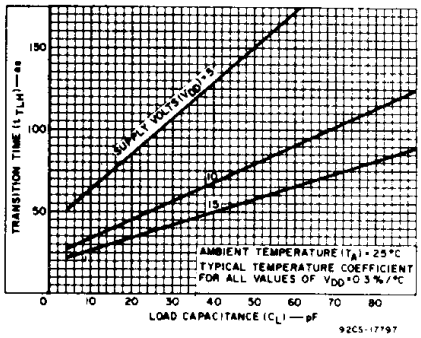



*Fig. 14 – Typical low-to-high transition time vs. $C_L$.*

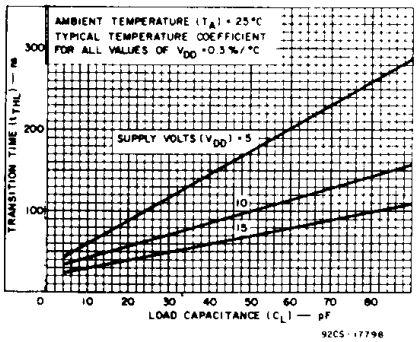



*Fig. 15 – Typical high-to-low level transition time vs. $C_L$ – CD4011A & CD4023A.*

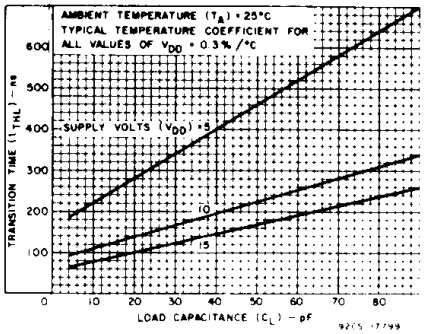



*Fig. 16 – Typical high-to-low level transition time vs. $C_L$ – CD4012A.*

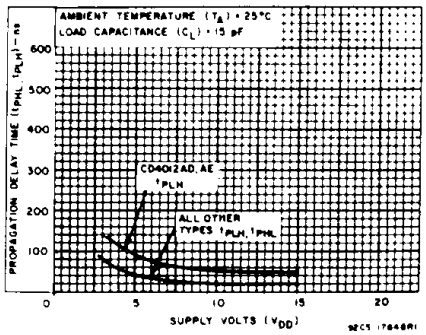



*Fig. 17 – Minimum propagation delay time vs. $V_{DD}$.*

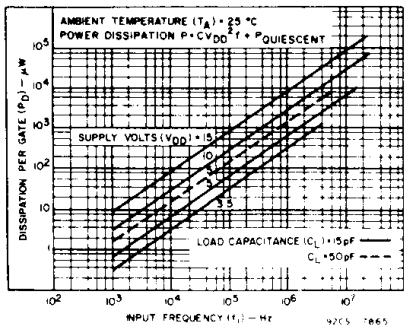



*Fig. 18 – Typical dissipation characteristics.*

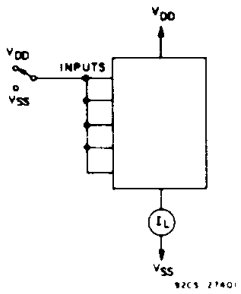



*Fig. 19 – Quiescent device current test circuit.*

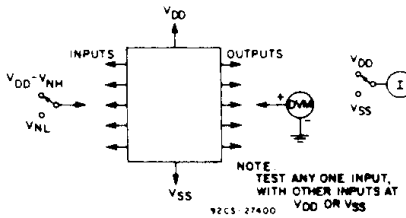



*Fig. 20 – Noise immunity test circuit.*

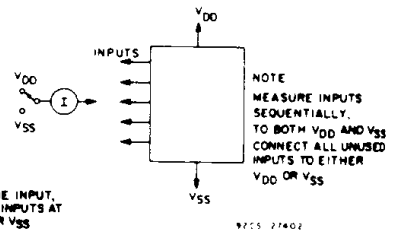



*Fig. 21 – Input leakage current test circuit.*

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD4011AD3 | ACTIVE | CDIP SB | JD | 14 | 1 | Non-RoHS & Non-Green | AU | N / A for Pkg Type | -55 to 125 | CD4011AD3 | Samples |
| JM38510/05001BCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 05001BCA | Samples |
| M38510/05001BCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 05001BCA | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

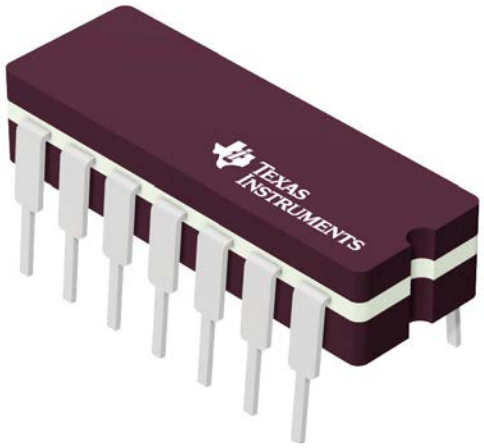
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# GENERIC PACKAGE VIEW

## J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

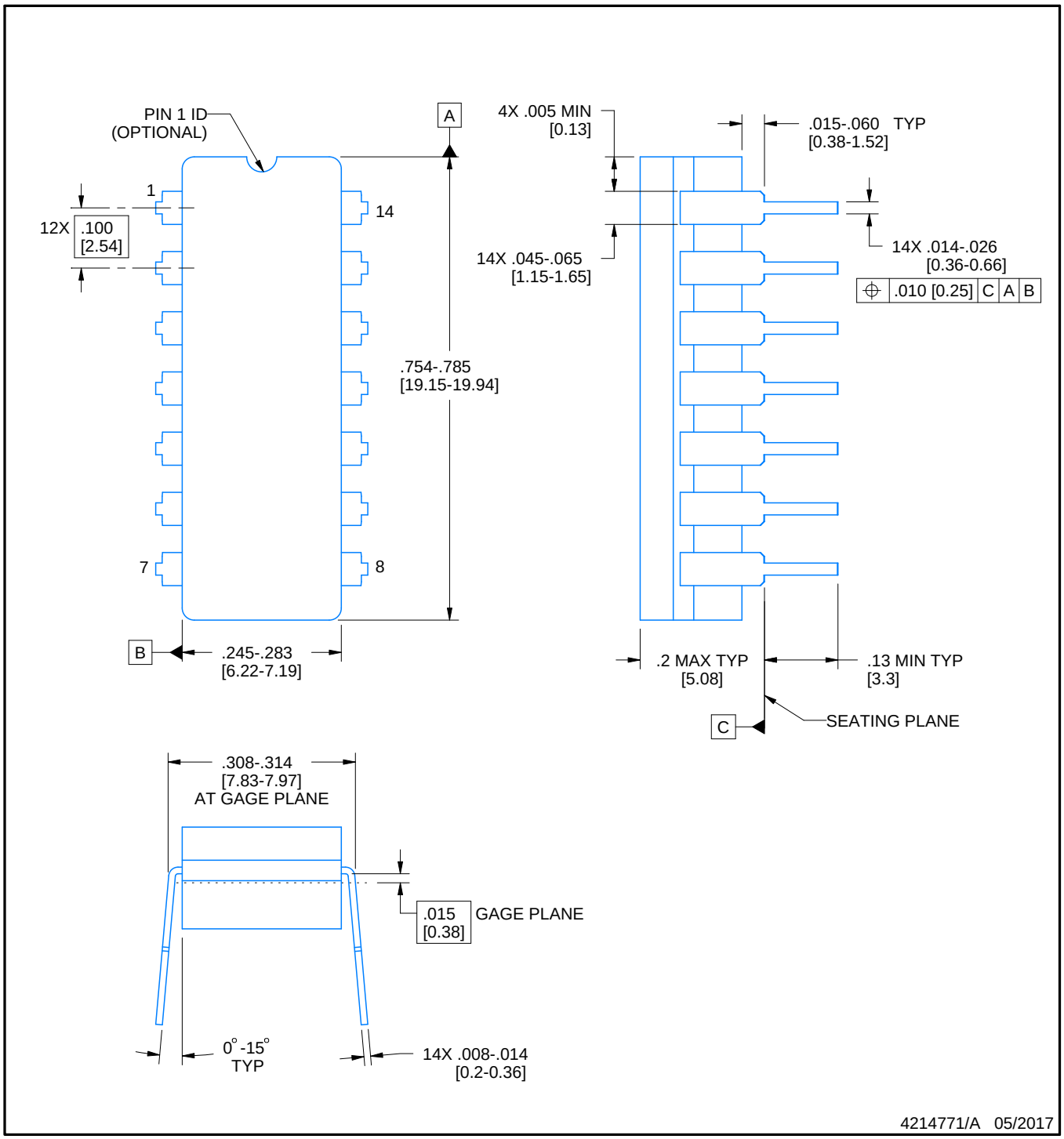
4040083-5/G

# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

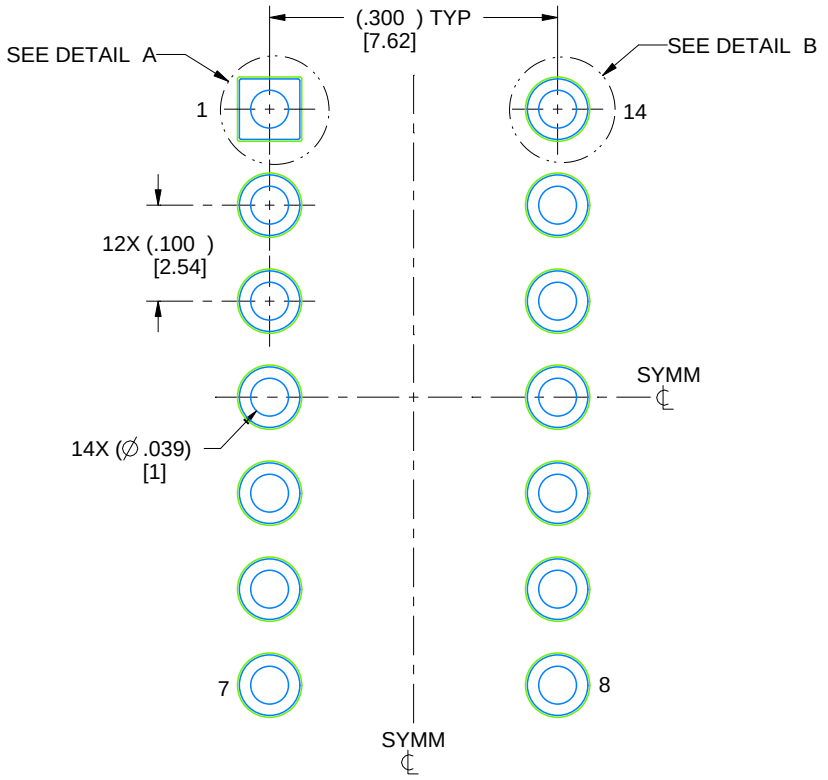
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

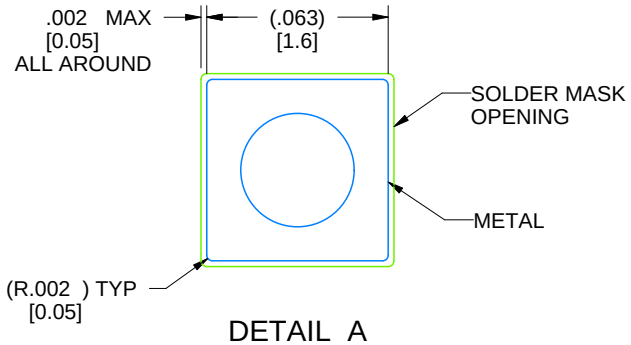
## J0014A

## CDIP - 5.08 mm max height

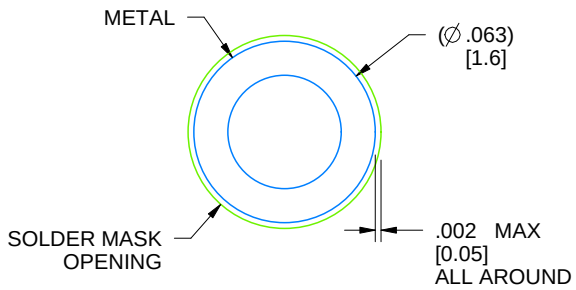
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



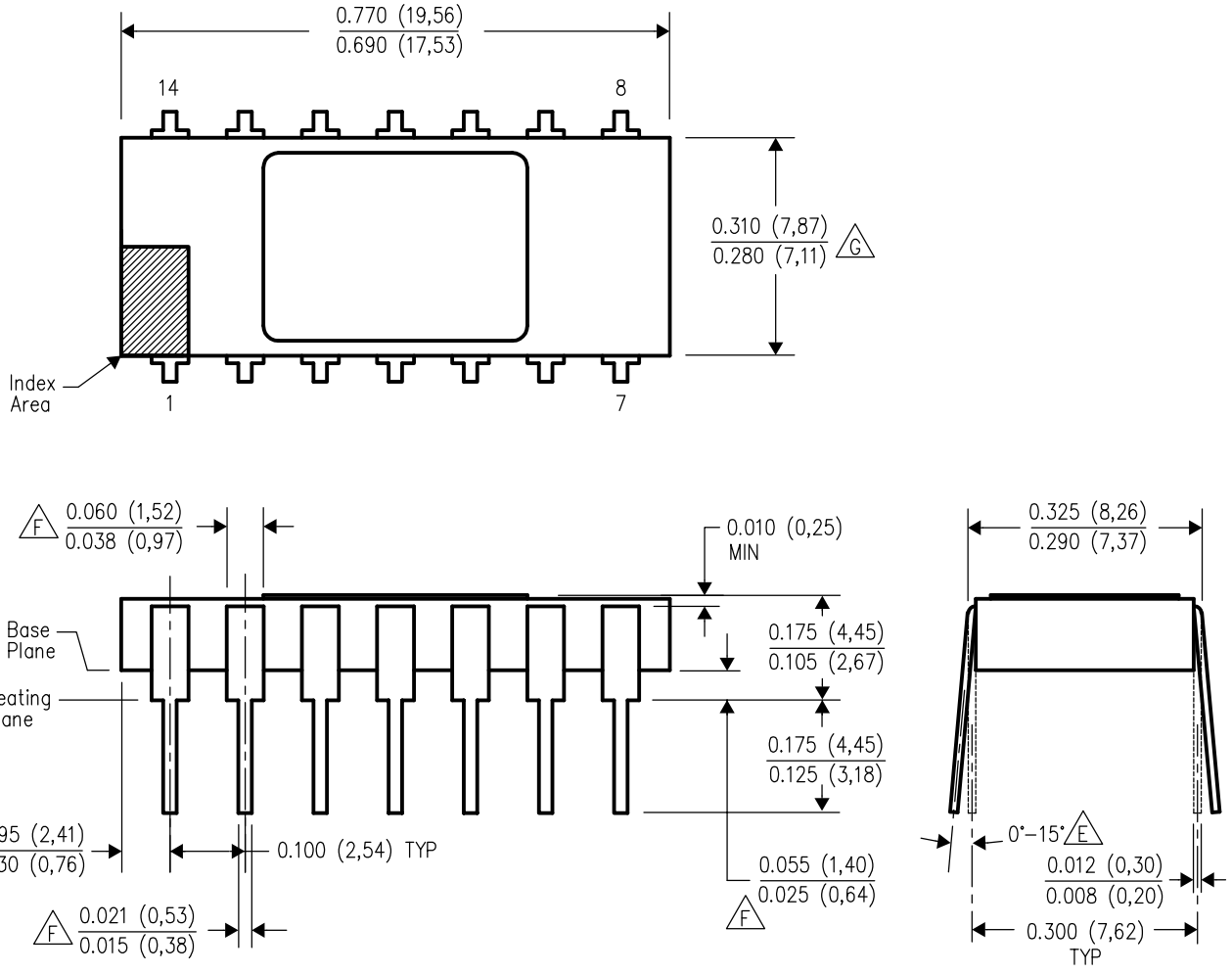

DETAIL A
SCALE: 15X




DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

## JD (R–CDIP–T14) CERAMIC SIDE–BRAZE DUAL–IN–LINE




NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Controlling dimension: inch.
- D. Leads within 0.005 (0,13) radius of true position (TP) at gage plane with maximum material condition and unit installed.
- E Angle applies to spread leads prior to installation.
- F Outlines on which the seating plane is coincident with the plane (standoff = 0), terminals lead standoffs are not required, and lead shoulder may equal lead width along any part of the lead above the seating/base plane.
- G Body width does not include particles of packing materials.
- H. A visual index feature must be located within the cross–hatched area.

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